Claims

[c1] 1. A semiconductor integrated circuit device for being put to a delay test using a scan path test circuit incorporated therein for a scan path test, comprising:
a two-pulse generator for generating two pulses spaced from each other by a pulse interval equal to a period of a test clock for the delay test which is input from an external source, from said test clock, and supplying the generated two pulses to the scan path test circuit.

[c2] 2. A semiconductor integrated circuit device according to claim 1, further comprising:
a PLL circuit for multiplying a frequency of said test clock and supplying a signal having the multiplied-frequency to said two-pulse generator.

[c3] 3. A semiconductor integrated circuit device according to claim 1, wherein said two-pulse generator comprises:
a gate signal generator for generating a gate signal to extract two pulses from said test clock; and
a latch gate circuit for outputting two pulses from said test clock according to said gate signal.

[c4] 4. A semiconductor integrated circuit device according to claim 2, wherein said two-pulse generator comprises:
a gate signal generator for generating a gate signal to extract two pulses from said test clock; and
a latch gate circuit for outputting two pulses from said test clock according to said gate signal.

[c5] 5. A device for testing a semiconductor integrated circuit device for being put to a delay test using a scan path test circuit incorporated in the semiconductor integrated circuit device for a scan path test, comprising:
a test board on which a semiconductor integrated circuit device to be tested is removably mounted; and
a two-pulse generator mounted on said test board, for generating two pulses spaced from each other by a pulse interval equal to a period of a test clock for the delay test, from said test clock, and supplying the generated two pulses to

the scan path test circuit.

[c6] 6. A device according to claim 5, further comprising:
a PLL circuit mounted on said test board, for multiplying a frequency of said test clock and supplying a signal having the multiplied-frequency to said two-pulse generator.

[c7] 7. A device according to claim 5, further comprising:
a clock generator for outputting said test clock.

[c8] 8. A device according to claim 6, further comprising:
a clock generator for outputting said test clock.

[c9] 9. A device according to claim 5, said two-pulse generator comprises:
a gate signal generator for generating a gate signal to extract two pulses from said test clock; and
a latch gate circuit for outputting two pulses from said test clock according to said gate signal.

[c10] 10. A device according to claim 6, said two-pulse generator comprises:
a gate signal generator for generating a gate signal to extract two pulses from said test clock; and
a latch gate circuit for outputting two pulses from said test clock according to said gate signal.

[c11] 11. A device according to claim 7, said two-pulse generator comprises:
a gate signal generator for generating a gate signal to extract two pulses from said test clock; and
a latch gate circuit for outputting two pulses from said test clock according to said gate signal.

[c12] 12. A device according to claim 8, said two-pulse generator comprises:
a gate signal generator for generating a gate signal to extract two pulses from said test clock; and
a latch gate circuit for outputting two pulses from said test clock according to said gate signal.

[c13] 13. A device according to 5, further comprising:
a frequency divider mounted on said test board, for dividing a frequency of said test clock into a frequency which can easily be measured.

[c14] 14. A device according to 6, further comprising:
a frequency divider mounted on said test board, for dividing a frequency of said test clock into a frequency which can easily be measured.

[c15] 15. A device according to 7, further comprising:
a frequency divider mounted on said test board, for dividing a frequency of said test clock into a frequency which can easily be measured.

[c16] 16. A device according to 8, further comprising:
a frequency divider mounted on said test board, for dividing a frequency of said test clock into a frequency which can easily be measured.

[c17] 17. A device according to 9, further comprising:
a frequency divider mounted on said test board, for dividing a frequency of said test clock into a frequency which can easily be measured.

[c18] 18. A device according to 10, further comprising:
a frequency divider mounted on said test board, for dividing a frequency of said test clock into a frequency which can easily be measured.

[c19] 19. A device according to 11, further comprising:
a frequency divider mounted on said test board, for dividing a frequency of said test clock into a frequency which can easily be measured.

[c20] 20. A device according to 12, further comprising:
a frequency divider mounted on said test board, for dividing a frequency of said test clock into a frequency which can easily be measured.

[c21] 21. A device for testing a semiconductor integrated circuit device, comprising:
a test board on which a semiconductor integrated circuit device according to claim 1 is removably mounted; and
a clock generator mounted on said test board, for outputting said test clock.

[c22] 22. A device for testing a semiconductor integrated circuit device, comprising:
a test board on which a semiconductor integrated circuit device according to claim 2 is removably mounted; and
a clock generator mounted on said test board, for outputting said test clock.

[c23] 23. A device for testing a semiconductor integrated circuit device, comprising:
a test board on which a semiconductor integrated circuit device according to claim 3 is removably mounted; and
a clock generator mounted on said test board, for outputting said test clock.

[c24] 24. A device for testing a semiconductor integrated circuit device, comprising:
a test board on which a semiconductor integrated circuit device according to claim 4 is removably mounted; and
a clock generator mounted on said test board, for outputting said test clock.

[c25] 25. A device according to claim 21, further comprising:
a second PLL circuit mounted on said test board, for multiplying a frequency of said test clock and supplying a signal having the multiplied-frequency to said semiconductor integrated circuit device.

[c26] 26. A device according to claim 22, further comprising:
a second PLL circuit mounted on said test board, for multiplying a frequency of said test clock and supplying a signal having the multiplied-frequency to said semiconductor integrated circuit device.

[c27] 27. A device according to claim 23, further comprising:
a second PLL circuit mounted on said test board, for multiplying a frequency of said test clock and supplying a signal having the multiplied-frequency to said semiconductor integrated circuit device.

[c28] 28. A device according to claim 24, further comprising:
a second PLL circuit mounted on said test board, for multiplying a frequency of said test clock and supplying a signal having the multiplied-frequency to said semiconductor integrated circuit device.

[c29] 29. A device according to claim 21, further comprising:

a frequency divider mounted on said test board, for dividing a frequency of said test clock into a frequency which can easily be measured.

[c30] 30. A device according to claim 22, further comprising:
a frequency divider mounted on said test board, for dividing a frequency of said test clock into a frequency which can easily be measured.

[c31] 31. A device according to claim 23, further comprising:
a frequency divider mounted on said test board, for dividing a frequency of said test clock into a frequency which can easily be measured.

[c32] 32. A device according to claim 24, further comprising:
a frequency divider mounted on said test board, for dividing a frequency of said test clock into a frequency which can easily be measured.

[c33] 33. A device according to claim 25, further comprising:
a frequency divider mounted on said test board, for dividing a frequency of said test clock into a frequency which can easily be measured.

[c34] 34. A device according to claim 26, further comprising:
a frequency divider mounted on said test board, for dividing a frequency of said test clock into a frequency which can easily be measured.

[c35] 35. A device according to claim 27, further comprising:
a frequency divider mounted on said test board, for dividing a frequency of said test clock into a frequency which can easily be measured.

[c36] 36. A device according to claim 28, further comprising:
a frequency divider mounted on said test board, for dividing a frequency of said test clock into a frequency which can easily be measured.